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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): B. CHANDRAN ET AL.

Serial No.: 10/023,819

Filed: December 21, 2001

For: CHIP-JOIN PROCESS TO REDUCE ELONGATION MISMATCH BETWEEN THE ADHERENTS AND SEMICONDUCTOR PACKAGE MADE THEREBY

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 & §1.98

Assistant Commissioner of Patents
Washington, D.C. 20231

January 18, 2002

Sir:

The Examiner's attention is directed to commonly assigned, copending application Serial No. 10/023,723 by the same inventors as the above-identified application, entitled "Semiconductor Package With Low Resistance Package-To-Die Interconnect Scheme For Reduced Die Stresses".

Respectfully submitted,

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